Parameter optimization of the T5TEA–ASIC for the Cherenkov Telescope Array

Bachelorarbeit aus der Physik

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15.12.2016

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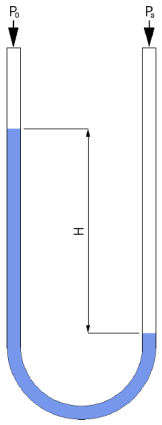
Abstract

Highly integrated electronic circuits have been developed to further increase the performance and energy efficiency of scientific measuring instruments. The Cherenkov Telescope Array (CTA) is one of the more recent scientific projects in astoparticle physics. It will improve upon the sensitivity of previous Cherenkov telescopes such as H.E.S.S., MAGIC or VERITAS by one order of magnitude. Thus, the readout electronics within the telescope cameras must be further developed. The TARGET module is an integral part of the two proposed camera designs of the Compact High Energy Camera (CHEC) and that of pSCT, responsible for triggering, sampling and the digitization of Cherenkov–flashes. The newest generation of this module features two dedicated Application Specific Integrated Circuits (ASICs), T5TEA for the trigger path and TARGET C (TC) for the data path. This thesis is concerned with the performance of T5TEA which features many different adjustable parameters. These influence the minimal achievable trigger threshold and the noise performance for an incoming signal. A systematic search for the best parameter values is performed. The newly found parameter values do not only provide a minimal threshold of $\mu \approx 2.54\,\mathrm{mV}$ and noise of $\sigma \approx 0.44\,\mathrm{mV}$ at 50 % trigger–efficiency but also slightly lower the power consumption of T5TEA. Furthermore, a variation of the threshold up to $\mu = \pm 0.23\,\mathrm{mV}$ on a daily basis was found.

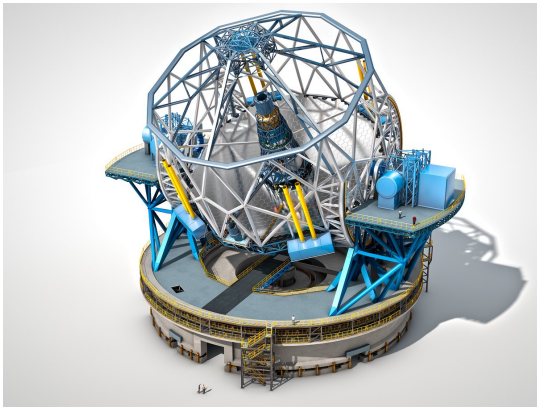
Contents

1 Introduction

Our present understanding of physics is based on the formulation of hypotheses which can be confirmed by measurements. Thus, measurements have been and always will be an integral part of physics. To proof a given hypothesis, specialized measuring instruments are devised and built. These can be very specific to the application area and examples can be found everywhere in science, ranging from a simple pressure gauge (see Figure 1a) to high–tech telescopes which observe the most distant stars like the Extremely Large Telescope (ELT) (see Fig. 1b).



(a) Schematic of a U tube differential pressure gauge [1].



(b) Design of the Extremely Large Telescope (ELT) [2].

Figure 1: Two application specific scientific instruments.

Nowadays most scientific measuring instruments are based on electronic circuits. The latter can be highly integrated which leads to a compact, energy efficient design reducing the overall cost. One of the newest instruments of this kind is the TeV Array Readout with GSa/s sampling and Event Trigger (TARGET) [3], developed for the Cherenkov Telescope Array (CTA). An introduction to CTA and TARGET is given in the upcoming chapters.

2 Cherenkov Telescope Array

CTA is a planed observatory, which components are currently evaluated. It aims to detect gamma rays with energies between 20 GeV and 300 TeV. For Very High Energy (VHE) gamma rays (energies > 100 GeV), this is easily done using Cherenkov–flashes caused by the interaction of these gamma rays with the atmosphere [4, 5].

2.1 Cherenkov–flashes and their detection

When a VHE photon hits the atmosphere, an electron–positron (e^+e^-) pair can be created due to interaction of the photon with the electromagnetic fields of atmospheric nuclei. These new particles emit photons by bremsstrahlung[1].

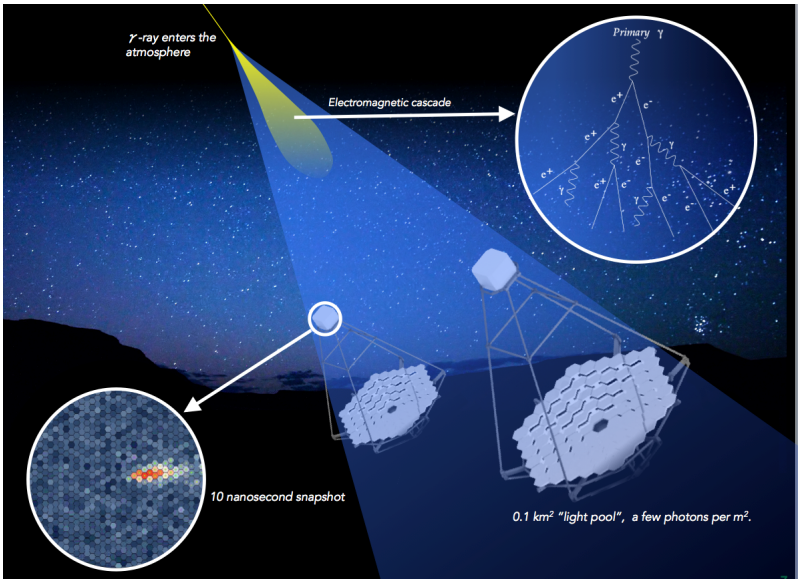


Figure 2: Illustration of an air shower caused by a photon [7].

The resulting photons can again create e^+e^- pairs. This so called electromagnetic cascade continues until the energy of the created bremsstrahlung photons is no longer sufficient to create further pairs. Thus, the so called air–shower, as seen in Figure 2, stops.
Due to the initial energy of the VHE photon, the electrons/positrons can travel through the atmosphere faster than the local speed of light ($c = \frac{c_0}{n}$)[2] [8].
This causes the emission of bluish Cherenkov–light which can be detected on the ground by Imaging Air Cherenkov Telescopes (IACTs). As seen in Figure 2, the light is focused onto a plane of photosensors by a mirror. Arrays of IACTs are used to increase sensitivity, energy resolution and improve background rejection, when the initial photon energy is

[1] Bremsstrahlung defines the emission of a photon by a charged particle due to rapid deceleration in matter [6, p. 254].

[2] c_0 is the speed of light in a vacuum; n is the refractive index of the surrounding medium.

reconstructed using the Cherenkov–light. Also the origin of the VHE photon can be determined. Since the timescale of these shower emissions are rather short ($\gtrsim 5\,\mathrm{ns}$ [9]), they are referred to as Cherenkov–flashes [4, 8, 5].

2.2 Overview

CTA will improve upon the sensitivity of current IACT arrays such as H.E.S.S., MAGIC or VERITAS by an order of magnitude. Two array sides are planned for CTA. One on the northern (La Palma, Spain) and one on the southern hemisphere (Paranal, Chile), to cover the entire sky [10, 7].

2.3 Proposed telescope designs

Due to the indirect proportional relationship between the gamma–flux and –energy, CTA is composed of different types of telescopes to cover the above-mentioned energy range [10, 7].

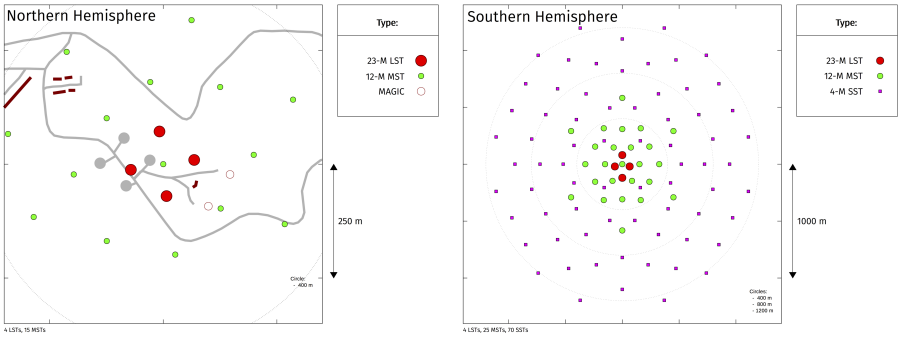


Figure 3: Proposed array layout for the northern and southern hemisphere [7].

The proposed CTA array layout can be seen in Figure 3 above. It features four Large Size Telescopes (LSTs) and 15 Medium Size Telescopes (MST) on the northern, as well as four LSTs, 25 MSTs and 70 Small Size Telescopes (SSTs) on the southern hemisphere [11, 12, 13].

Large Size Telescopes

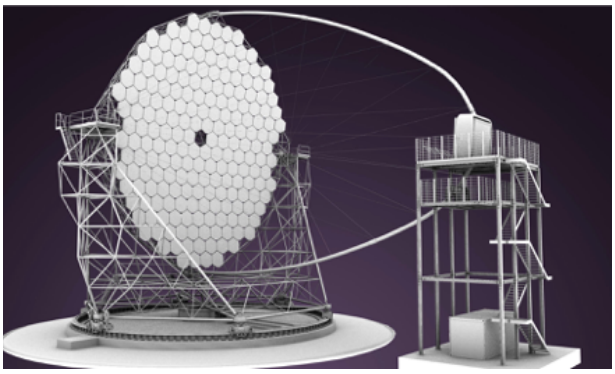
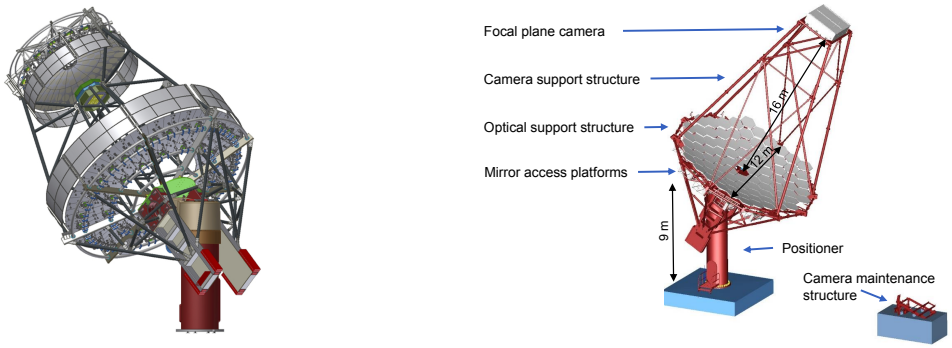


Figure 4: 3D model of the LST [11].

The LSTs provide coverage for the low gamma–ray energy range between 20 GeV – 200 GeV. Due to the relatively low gamma–ray photon energies, the created Cherenkov–flashes are rather dim. Thus, a large mirror with a diameter of 23 m is needed to collect enough light. However, in this energy range the gamma–ray flux is large and only few of these telescopes are needed to observe enough Cherenkov–flashes. The first LST is currently being built on La Palma [11].

Medium Size Telescopes



(a) Schwarzschild–Couder telescope design (pSCT) [10].

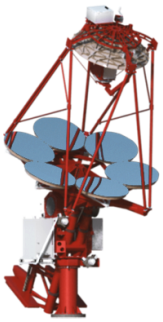
(b) Modified Davies–Cotton telescope design [12].

Figure 5: Proposed designs for MSTs.

The MSTs are built for the energy range between 100 GeV – 10 TeV. Two designs have been proposed. A Modified Davies–Cotton telescope (see Figure 5b), featuring a mirror

with 12 m in diameter consisting of hexagonal panels and a Schwarzchild–Couder Telescope (pSCT) (see Fig. 5a). The pSCT is a dual–mirror design with a primary and secondary mirror diameter of 9.7 m and 5.4 m respectively [10, 12].

Small Size Telescopes



(a) GCT design.

(b) ASTRI design.

(c) SST-1M design.

Figure 6: Proposed designs for SSTs [13, 7].

The remaining energy range from a few TeV up to 300 TeV is covered by the SSTs. Because the flux of gamma–ray photons declines with increasing energy, Cherenkov–flashes are rather rare but bright. Thus, a higher number of SSTs with small mirrors and a large spacing between them is required to capture enough events (compare Fig. 3).
The proposed designs, as shown in Figure 6, include again a Davies–Cotton design (SST–1M) proposed by Swiss and Polish institutions with a 4 m diameter mirror. Also the Gamma Cherenkov Telescope (GCT) and Astrophysics con Specchi a Tecnologia Replicante Italiana (ASTRI) which are a Schwarzschild–Couder designs (see Fig. 6), have been proposed. Both feature a secondary 2 m diameter mirror. The diameters of the primary mirrors of GCT and ASTRI are 4 m and 4.3 m respectively [13, 14, 15].

2.4 Cameras featuring TARGET

The cameras featuring TARGET are implemented in the GCT design for the SST and the pSCT design for the MST. The Compact High Energy Camera (CHEC) has been designed for the GCT. The CHEC–M model features Multi Anode Photo Multipliers (MAPMs) as photosensors. A model of CHEC–M can be found in Figure 7 below.

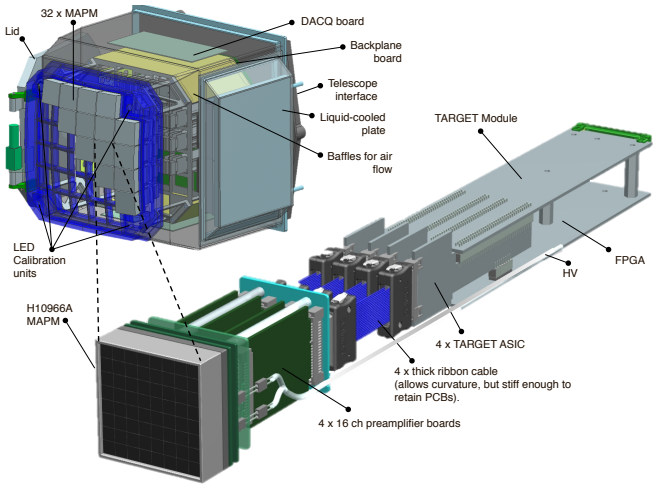


Figure 7: CHEC–M design and a front end electronics (FEE) module [16].

CHEC–M is equipped with 32 MAPMs, each having 64 pixel/channels with a size of $6 \times 6\,\mathrm{mm}^2$, accounting for $2,048$ pixels in total of which pairs of four form a so called superpixel. Behind each MAPM, four 16 channel preamplifier boards shape[3] the signal of each channel for optimal processing.

Four TARGET Application–Specific Integrated Circuits (ASICs) with 16 channels each, receive the shaped and amplified signals. Here the superpixels are formed via analog sum of four channels. The trigger signal of each superpixel is sent to the backplane[4]. A trigger from one superpixel corresponds to a level one trigger. Only when two neighboring superpixels trigger within a specified coincidence time, a level two trigger and thus a camera wide readout request is sent by the backplane. An Field Programmable Gate Array (FPGA) which also controls settings of the TARGET ASICs, prepares the data packages and sends them. The data acquisition (DACQ) board serves as a network switch. Additionally, a newly developed CHEC–S camera replaces the MAPMs with Silicon Photomultipliers (SiPMs) and a newer generation of TARGET is used [14, 17, 16, 18, 19].
The signal processing of the pSCT camera, besides using a different preamplifier, functions similar to the CHEC–S design. Each module contains 64 SiPMs which are grouped together in groups of four to form pixels of $6.5 \times 6.5\,\mathrm{mm}^2$ in size. Containing nine fields of 25 modules in total, this accounts to $11,328$ channels.

Since TARGET is such a critical camera component and has a significant impact on the telescopes performance, an optimization of the internal mechanisms is of great use.

[3] Full width at half maximum (FWHM) $5.5 - 10.5\,\mathrm{ns}$ with an edge time between $3.5 - 6.0\,\mathrm{ns}$ [16].
[4] The backplane refers to the PCB in which the FEE module is plugged into.

3 TARGET

TARGET is an Application–Specific Integrated Circuit (ASIC) designed to trigger, sample and digitize signals of Cherenkov cameras. TARGET is implemented in the proposed GCT design for the SST as well as the SCT design for the MST of CTA (see chapter 2.3 and 2.3) [3, 20, 21]. TARGET is designed to meet the requirements, set by the CTA consortium. These include:

- Sampling rate ≥ 1 GSa/s, to sample Cherenkov–flashes of $\gtrsim 5$ ns.
- Dynamic range ≥ 10 bit for analog to digital conversion in read out.
- Should be able to trigger signals $\leq 10\,\mathrm{mV}$ [22].
- Deep analog buffer for sample storage.
- Short dead time.

Many improvements to this design were made, resulting in different TARGET generations. This thesis is concerned with the latest generation up to now. While in previous generations triggering and sampling were handled in one ASIC, these two functions are now separated into T5TEA (trigger path) and TARGET C (TC) (data path) respectively. This reduces interferences inflicted upon the trigger path by the data path [20, 21]. A TARGET–evaluation board, as seen in Figure 8 below, was used for all upcoming measurements. This evaluation board provides a framework to test T5TEA, TC and the FPGA. Unlike the finished module, the evaluation board grants access to test points on the PCB itself as well as different components, which may later on be too tightly integrated.

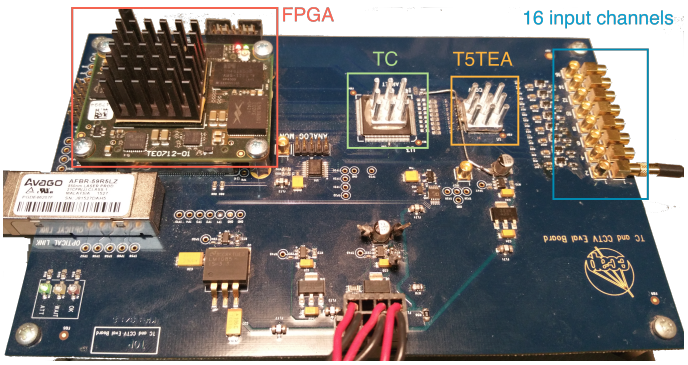


Figure 8: TARGET–evaluation board with FPGA, TC and T5TEA.

3.1 TARGET C

An arriving signal is sampled using a sampling array consisting of two 32–cell switched–capacitor array blocks operated in ping–pong fashion. Thus, while one block is sampling the signal, the contents of the other block can be transfered into the deep buffer. This provides continuous sampling without dead time.
The deep buffer consists of $16,384$ switched–capacitor cells, divided into 64 columns and 8 rows of 32–cell blocks. Assuming 1 GSa/s this provides ≈ 16 µs of buffer time.

When a trigger signal is applied (either by T5TEA or external sources), random blocks of 32–cells in the deep buffer can be read out simultaneously for each channel via Wilkinson analog–to–digital converters (ADCs). They work by starting a voltage ramp and a 12 bit counter at the same time. When the voltage of the ramp is equal to the voltage stored in the cell, the counter stops. This 12 bit value represents the digitized value. It should be noted that a trigger signal forces a read out of all channels.
Since there have been no significant changes in terms of operation between TC and the previous generation TARGET 7, an illustration of the sampling process described above can be found in Figure 9 [9].

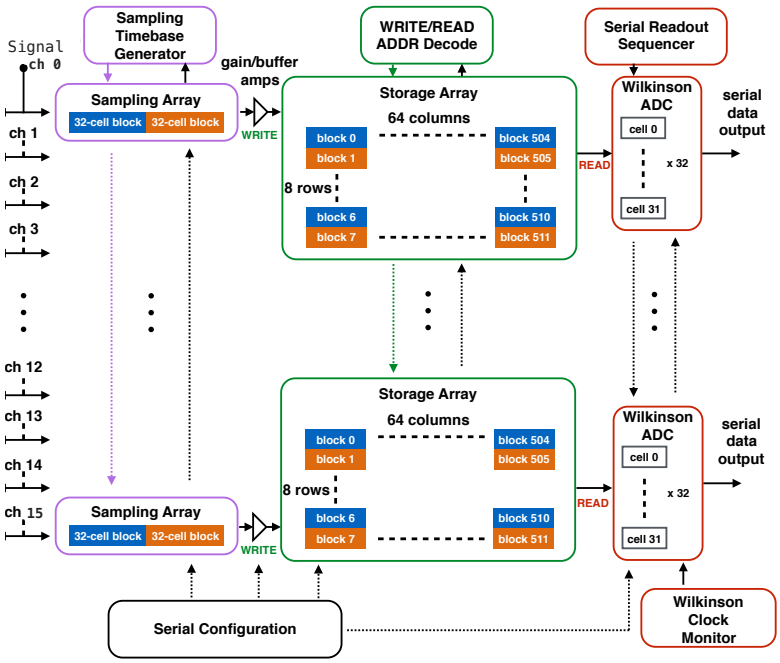


Figure 9: Functional block diagram of TARGET 7 (modified by the author) [21].

3.2 T5TEA

Signals of the photo sensors are amplified and shaped before they are forwarded to the 16 input channels of the TARGET ASIC (see chapter 2.3). Those signals are then grouped together in groups of four to form so called trigger–groups by using an analog sum. The summed up signal is compared to a trigger–threshold via a comparator. When the trigger–threshold is crossed, a trigger signal is produced by T5TEA.
This signal is forwarded to an FPGA on the TARGET–evaluation board (see Fig. 8) which can initiate the data read out in TC. An illustration of a successful trigger can be seen in Figure 10. Here, the signal noise is mainly introduced by the evaluation board itself [22].

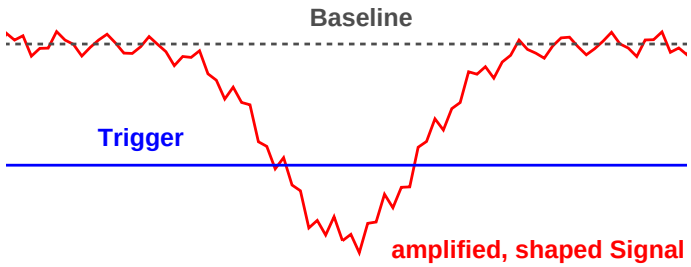


Figure 10: Illustration of the amplified, shaped and summed up signal position relative to the trigger in order to achieve triggering (with indicated signal noise).

The baseline in Figure 10 is produced, when no signal is applied (also affected by board internal noise).
In order to setup T5TEA to produce the desired trigger behavior, many parameters can be modified. These are set by the FPGA in 12–bit Digital–to–Analog Converter counts (DAC–counts) between $0 - 4095$ corresponding to a voltage range of $0\,\mathrm{V} - 2.5\,\mathrm{V}$. However, all parameters should be chosen within $900 - 3000$ DAC–counts to maintain stability.

The most vital parameters for successful triggering are:

- **Vped_ChNR**[5]: Controls a channel dependent offset on the signal. Looking at Figure 10, an increase in Vped shifts the signal down, towards the trigger.

- **PMTref4_TrGp**[6]: Controls a trigger–group dependent offset on the signal. Again looking at Figure 10, an increase in PMTref4 shifts the signal upwards and away from the trigger. Therefore, counteracting Vped_ChNR.

- **TRG_Thres**: Controls the position of the trigger. An increase in this parameter would shift the trigger towards the signal (or baseline, when no signal is applied).

[5] **Ch**annel **N**umbe**r**.
[6] **Tr**igger **G**rou**p**.

These, however, are not all available parameters. The functions and effects of the remaining parameters on T5TEAs performance and their interplay with those listed above, will be investigated and explained in the following chapters.

4 Parameter optimization

The parameters of T5TEA, mentioned in chapter 3, and others have been previously varied to further improve performance of T5TEA. The attempts performed with the Trial–and–Error method lead to specific values for each parameter and are hereafter referred to as 'default value' (see appendix A.1) [23]. Now a systematic search for the best values of T5TEAs parameters is performed.
All measurements are carried out using input channel 0 with sampling (TC) enabled if not stated otherwise. Thus, the corresponding trigger–group or channel number for a given parameter is omitted.

4.1 Power consumption of T5TEA

One of the main concerns of a large scale structure such as the CTA is heat development caused by the overall compact electronic design. One way to counteract this is to minimize the current draw which can be measured for each component of the TARGET–evaluation board via measuring points on the board itself. However, only the current draw of T5TEA is considered within the scope of this thesis.
The only variable parameters that contribute to the current draw of T5TEA are the bias–parameters. These provide the bias of certain amplifiers in the T5TEA architecture. One expects the current draw to decrease with declining bias–values. This can be seen in Figure 11 below.

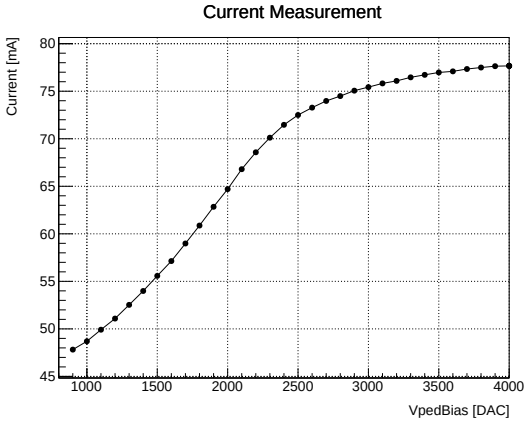


Figure 11: Current draw of T5TEA for default values and variable VpedBias.

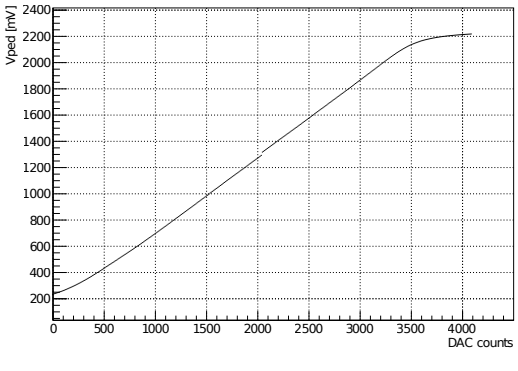


Figure 12: Example of a transfer–function for Vped_14 [23].

The shown bias–parameter in Figure 11 is VpedBias. The nature of this parameter will be discussed in the next chapter. In Figure 11 the graph flattens out at approximately 2300 DAC–counts. This is due to the available linear–range of the digital–to–analog converter for this parameter and the saturation of the amplifier that VpedBias provides the bias

for. The functional relationship between the entered DAC–value and the output voltage is described by the so called transfer–function. Despite corresponding to another parameter, the overall form shown in Figure 12 remains the same. The DAC–interval in which the transfer–function behaves linearly is called the linear–range.

Outside this interval the transfer–function flattens out, hence behaves non–linearly [23]. Since the current draw of the amplifiers is proportional to the bias voltage, the same flattening can be observed in the current measurement. Results for the other bias–parameters, which behave similarly, can be found in appendix A.2.

Due to the general trend throughout all bias–parameters, one can conclude that in oder to reduce power consumption in general it is better to choose lower bias–values if possible.

4.2 VpedBias

The first parameter to be optimized is VpedBias. It controls the supply bias for the channel dependent offset, determined by the Vped DAC–value. Default values for VpedBias and Vped are 1800 and 1000 respectively.
A change in VpedBias for constant Vped leads to a non–linear alteration of the offset voltage. This behavior is illustrated in Figure 13.

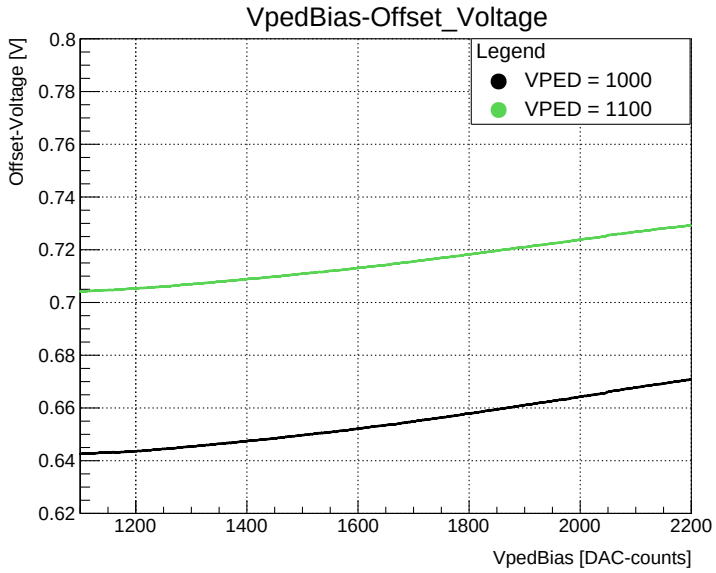


Figure 13: Offset voltage as a function of VpedBias for two Vped values.

In order to get valid parameters for the TARGET–evaluation board the offset voltage has to be $\geq 0.65\,\mathrm{V}$ for TC to function correctly [22]. As one can see in Figure 13 this is not always the case (depending on the set parameters). Therefore, Vped must be adjusted as

well to produce an acceptable offset voltage.

Ideally, for a given VpedBias the DAC–Value for Vped is simply increased until the measured offset voltage is equal to the offset voltage generated by the default values for both parameters (0.6572 V).

However, this is practically impossible because the DAC operates equivalent to a voltage divider. Therefore, the voltage step per DAC–count is dependent on the values and tolerances of the built–in resistors [23].
Thus, Vped is increased until the deviation between the measured offset voltage and that of the default values is minimal. The results can be found in Table 2 (appendix A.3.1).

To further analyze the trigger behavior caused by these parameters, the following measurements are introduced.

4.2.1 Trigger–efficiency measurement

For each full set of given parameters[7] a signal pulse with a frequency of $f_{\text{pulse}} = 1\,\text{kHz}$, FWHM of 10 ns, edge time[8] $t_{\text{edge}} = 5.4\,\text{ns}$ and varying amplitude is applied to the channel input. For the used function generator[9], an offset equal to the half amplitude has to be set to achieve the desired output amplitude.

The trigger-efficiency for any given amplitude is defined by:

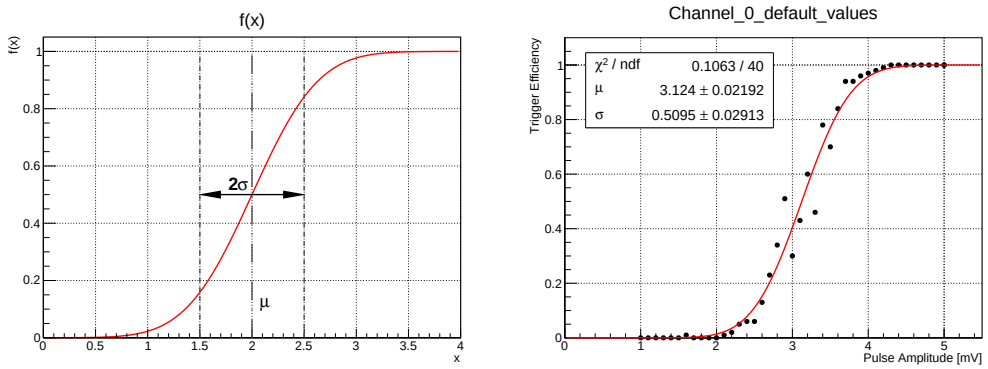
$$\epsilon = \frac{\text{Number of measured triggers}}{\text{Number of expected triggers}} = \frac{N_{\text{m}}}{N_{\text{e}}}. \tag{1}$$

The trigger–count is measured over a period of $\Delta t = 0.1\,\text{s}$. Thus, the expected value is given by the relation $N_{\text{e}} = f_{\text{pulse}} \cdot \Delta t = 100$. The measured trigger–count can be read out from the FPGA.
The signal amplitude is increased from $1\,\text{mV}_{\text{pp}}$ up to the point where at least seven times the trigger-efficiency of $\epsilon = 1$ (100 %) is measured. Then function 2 which resembles a Gaussian error function is fitted to the measured values (see Fig. 14b):

$$f(x) = \frac{1}{2}\text{erf}\left(\frac{x-\mu}{\sqrt{2}\sigma}\right) + \frac{1}{2}. \tag{2}$$

An exemplary plot of Function 2 can be found in Figure 14a. Here, μ resembles the voltage amplitude at which T5TEA is able to trigger with 50 % efficiency and will be further referred to as threshold. Since σ represents the width of the Gaussian error function, it is equivalent to and will be referred to as noise (see Figure 2).

[7] A full set of parameters refers to every possible parameter of T5TEA being set to a specific value.
[8] Rise time of the singal amplitude from 10 % to 90 %.
[9] Keysight 33611A, 80 MHz, 1–Channel, load impedance 50 Ω.



(a) Plot of function 2 ($\mu = 2$, $\sigma = 0.5$) with indicated parameter meaning.

(b) Trigger-efficiency measurement for the default values on channel 0 (PMTref4 = 1980, TRG_Thres = 2974) including fit–function (red) and measured values (black).

Figure 14: Illustration of a trigger–efficiency measurement.

4.2.2 PMTref4–trigger–rate measurement

For constant TRG_Thres, PMTref4 is varied without an applied signal. The trigger–rate is the measured trigger–count within 0.1 s. An example plot of this measurement can be found in Figure 15.

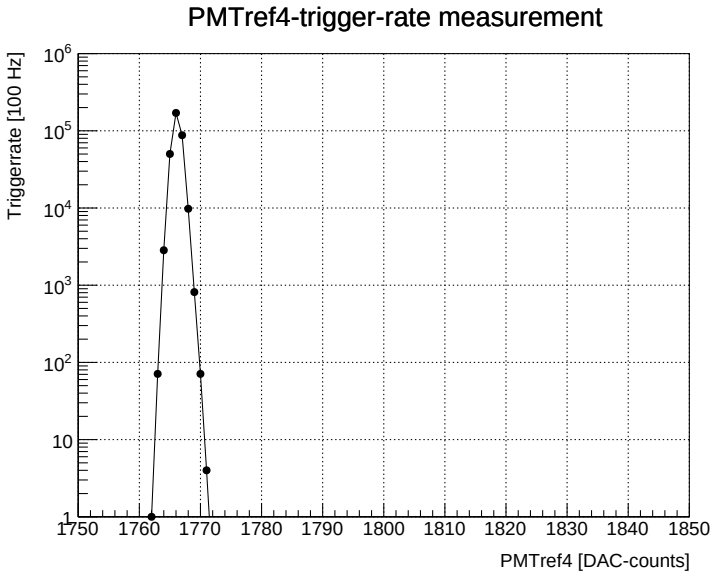


Figure 15: Trigger–rate measurement for TRG_Thres = 1050.

The significant increase in the trigger–rate at around 1760 DAC–counts is caused by the baseline (compare Fig. 10), which is affected by board internal noise, being shifted through the trigger by PMTref4. The point where no more triggers are measured after the first increase (approximately 1771 DAC–counts in Figure 15) is taken as the start value for PMTref4. After this point the trigger is no longer above or within the baseline and successful triggering can take place. Outside the baseline the trigger–rate is zero. However, due to the logarithmic scale in Figure 15 these values are not displayed within the plot.

4.2.3 PMTref4–TRG_Thres scan

To check how well the set parameter for VpedBias and Vped do perform, a scan through the PMTref4–TRG_Thres parameter space is performed.
As noted in chapter 3, these two parameters are vital for threshold and noise (compare chapter 4.2.1).

In the first part of this scan, a start value for PMTref4 is found using the PMTref4–trigger–rate measurement (see chapter 4.2.2).
From there on, PMTref4 is increased by one DAC–count five times. To get an overview how noise and threshold behave for higher PMTref4, the step size is then changed to 100 DAC–counts. Furthermore, the minimum threshold μ_{min} and the corresponding noise $\sigma_{(\mu_{\text{min}})}$ is taken from the measured data and added to the plot.

Especially the first values of the thresholds found after the PMTref4 start value are interesting. Here, the thresholds are the smallest for any given TRG_Thres. The results are filled into a histogram and plotted with a heat map. A PMTref4–TRG_Thres scan for VpedBias can be found in Figure 16 below.

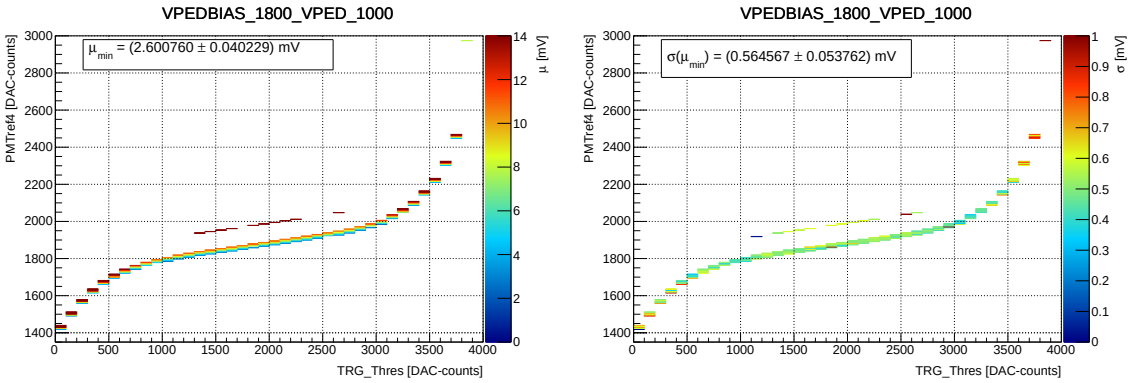


Figure 16: PMTref4–TRG_Thres Scan for VpedBias = 1800 and 1000.

To quantify the result further, the noise and threshold values for TRG_Thres between 1500 - 2500 DAC–counts are filled into histograms. As seen in Figure 16, this interval provides a predictable, linear behavior.

For those histograms the mean value as well as the RMS/$\sqrt{n-1}$ is determined and plotted. Here n represents the number of histogram entries and RMS the Root–Mean–Square of the histogram data, therefore providing a measure for the error of the determined mean value of the respective histogram.
For the noise, all values within the defined TRG_Thres interval are filled into the histogram. Whereas only the first (smallest) threshold value for each TRG_Thres value is filled into the threshold histogram. Hence, the development of the lowest possible threshold can be observed. The result of this can be found in Figure 17 below.

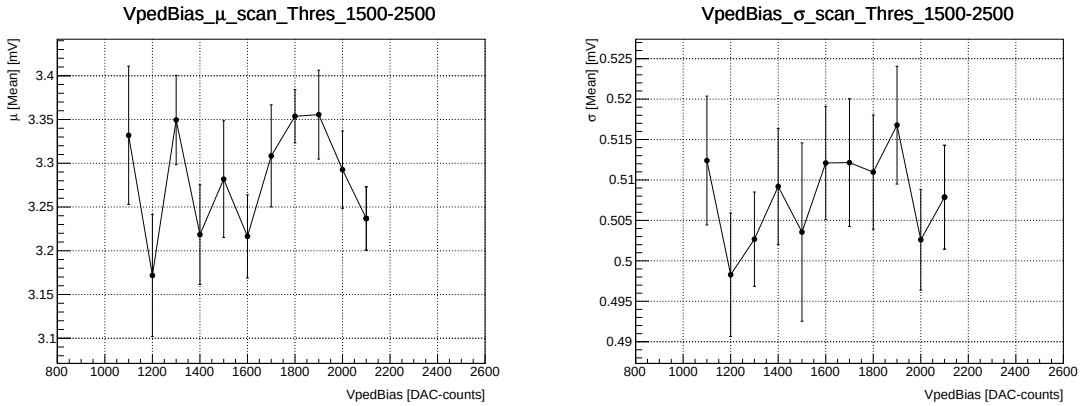


Figure 17: Result for threshold μ and noise σ of the VpedBias optimization.

As one can see in Figure 17, there are no significant changes in the noise or threshold with regard to the error. Thus, the default value for VpedBias (1800) can be maintained.
The value is not lowered as suggested by the found power consumption relation in chapter 4.1 because this is one of the few parameters that must have a certain value for TARGET to function properly [22].

4.3 Vped

Vped controls an offset that can be applied to each channel separately. It is studied between 900 - 1200 DAC–counts using a step size of 25 DAC–counts for TRG_Thres via a PMTref4–TRG_Thres scan. The step size of the scan was modified in order to acquire more information about the trigger behavior at higher thresholds. After the first five, the one DAC–count long steps are extended to five DAC–counts for the following five steps. Then the step size is changed again to 20 DAC–counts for the rest of the scan.
Important scans can be found in the appendix A.3.2.

Although Vped values lower than 1000 should not be used in conjunction with VpedBias = 1800 (compare chapter 4.2) for TC to function properly, they may become relevant if T5TEA is operated without TC in future use cases.

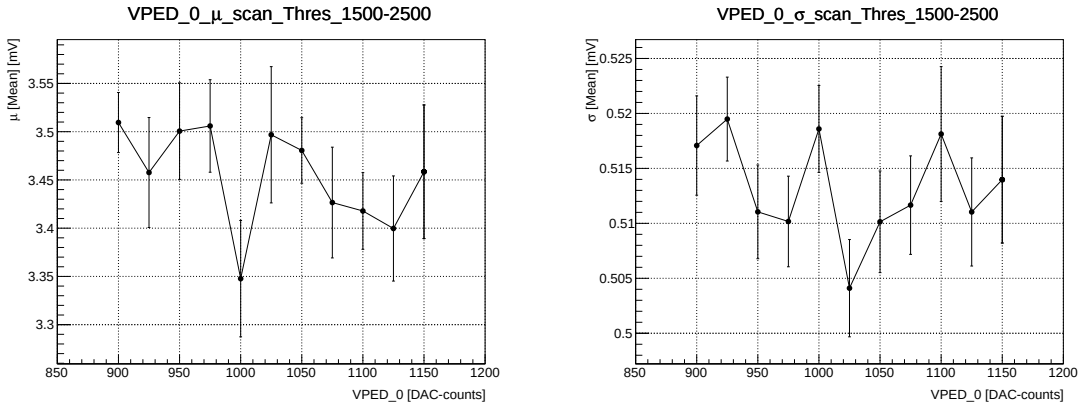


Figure 18: Result for threshold μ and noise σ of the Vped optimization.

As it can be seen in Figure 18, there are again no significant changes for threshold and noise. The observed minimum at 1000 DAC–counts is likely to be a statistical fluctuation. Therefore, the default value 1000 is maintained.

4.4 TRGsumbias

TRGsumbias controls the bias for the summing amplifiers of T5TEA for all trigger–groups. The summing amplifier works by comparing the trigger group depending offset, determined by PMTref4, to the trigger–group signal (Nsum), which consists of the analog sum of four input channels. The output is proportional to the difference of these two signals. Thus, leading to an inversion of the trigger–group signal and an offset proportional to the set PMTref4 value (compare Figure 10). The schematic of a summing amplifier can be found in Figure 19 below.

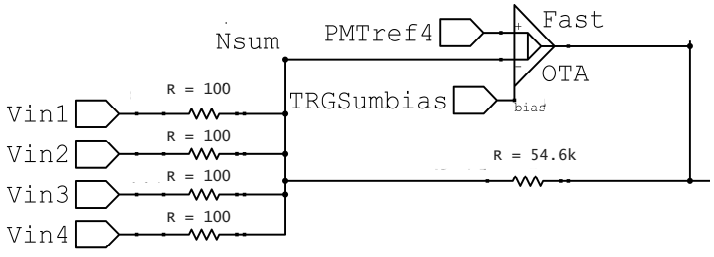


Figure 19: Schematic for a summing amplifier of T5TEA (modified by the author) [24].

For a sufficiently high bias, output of the amplifiers should be linear with the predetermined difference between PMTref4 and TRGsum. However, if the summing amplifier outputs a voltage that is not within a certain linear–range of the amplifier, it shows a non–linear behavior. Thus, a small offset change requires a larger change in PMTref4. This can be

seen in the right plot of Figure 20 for PMTref4 values lower 1700 and higher than 1950.

However, when the bias for the amplifier is rather low, the maximum voltage on the output of the amplifier is limited. Given an appropriate bias value the output voltage can be limited to the linear–range of the amplifier. Therefore, the non–linear offset behavior disappears. This behavior can be seen in the left plot of Figure 20.
TRGsumbias is studied between 900 - 2800 DAC–counts using the established PMTref4–TRG_Thres scan. Important scans can be found in the appendix A.3.3.

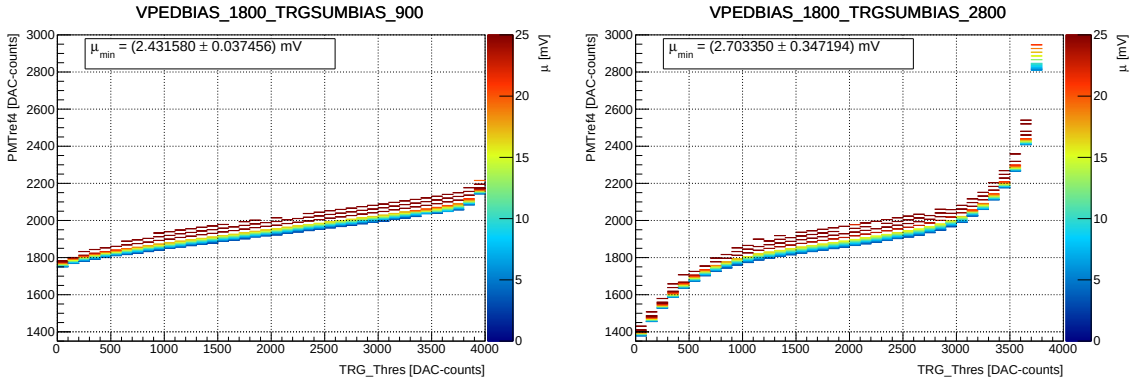


Figure 20: PMTref4–TRG_Thres scan for TRGsumbias = 900 and 2800.

In Figure 20 one can recognize the impact of the bias value on the PMTref4 offset linearity as descried above.

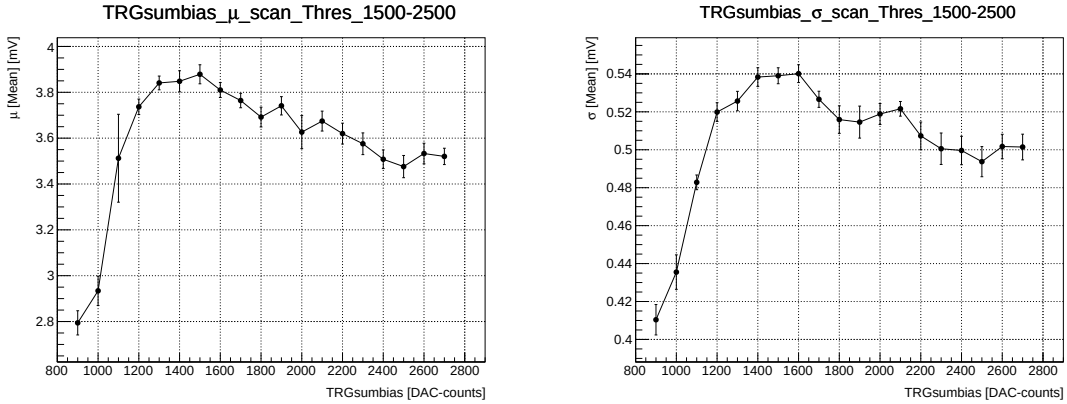


Figure 21: Result for threshold μ and noise σ of the TRGsumbias optimization.

The results, as seen in Figure 21, show a clear trend. The noise as well as the thresholds decrease rapidly for lower values. Within the measured range TRGsumbias = 900 seems to be the best possible choice. However, it must be noted that this is a rather low value

which is the minimum that should be used for any given parameter, as stated in chapter 3.2.

To check whether this also yields results that meet the requirements, two additional measurements are carried out. At first, the resulting trigger–range is checked in order to validate that it is possible to trigger on signals with amplitudes between 3 mV − 150 mV.

The PMTref4–TRG_Thres scan (see chapter 4.2.3) is altered so that threshold up to 1200 mV can be measured. Also the step size for PMTref4 is changed to a fixed value of 50 DAC–counts and the maximum value for the threshold is displayed instead of the lowest.

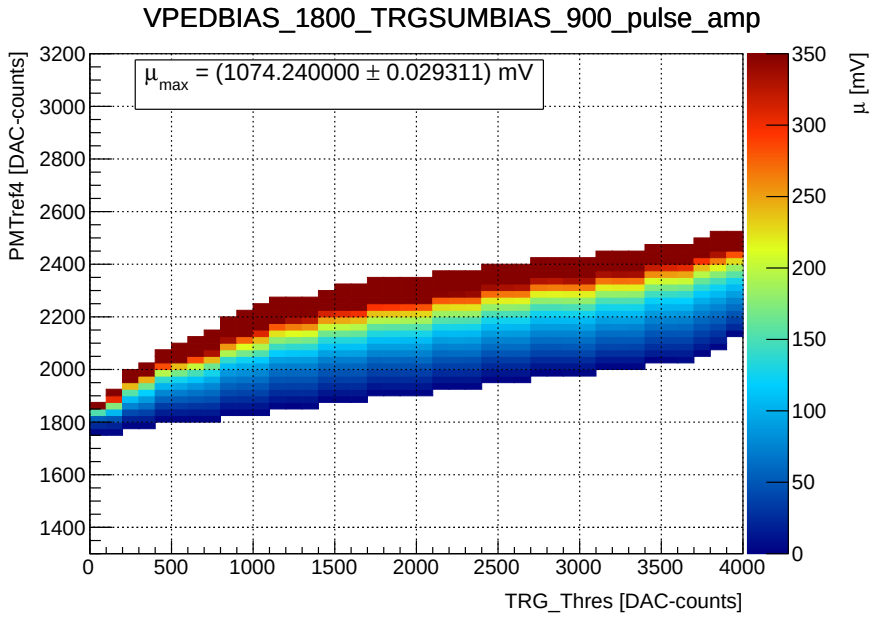


Figure 22: Test of the trigger–range for TRGsumbias = 900.

As one can see in Figure 22 thresholds of 150 mV (indicated in green) up to 1070 mV can be measured without any problem. It should be noted that the color code was restricted for thresholds up to 350 mV even though thresholds up to $\mu \approx 1074$ mV are filled into the histogram.

Finally, a measurement is conducted in order to observe the trigger-efficiency. It should not exceed acceptable values ($1 \leq \epsilon \leq 1.1$) for a big input signal amplitude when a low threshold is selected. The result can be seen in Figure 23 below.

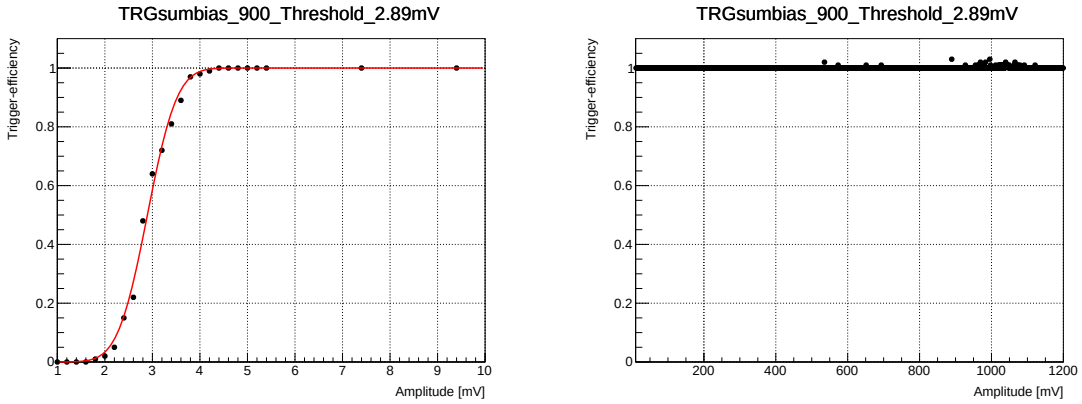


Figure 23: Trigger–efficiency for TRGsumbias = 900, amplitudes up to 1200 mV and a low threshold of $\mu = 2.89$ mV.

As illustrated in Figure 23, even amplitudes exceeding 500 mV produce acceptable trigger–efficiencies when a low threshold ($\mu = 2.89$ mV) is set.

It can be concluded, that for TRGsumbias = 900 T5TEA meets the established requirements while providing lower noise and thresholds. Therefore, this value is used from now on if not indicated otherwise.

4.5 Stability measurement

Comparing Figure 17 for VpedBias = 1800 ($\mu \approx 3.35$ mV) and Figure 21 for TRGsumbias = 2400 ($\mu \approx 3.5$ mV), one notices that the mean values for the threshold deviate even though the parameters are the same.
To investigate this further, another measurement was carried out. For PMTref4 = 1924 and TRG_Thres = 2000, fifty successive trigger–efficiency measurements are performed each day for 15 days. For each day the mean value for threshold and noise as well as their corresponding errors[10] are determined using histograms. The result can be seen in Figure 24 below.

[10] $\frac{RMS}{\sqrt{n-1}}$

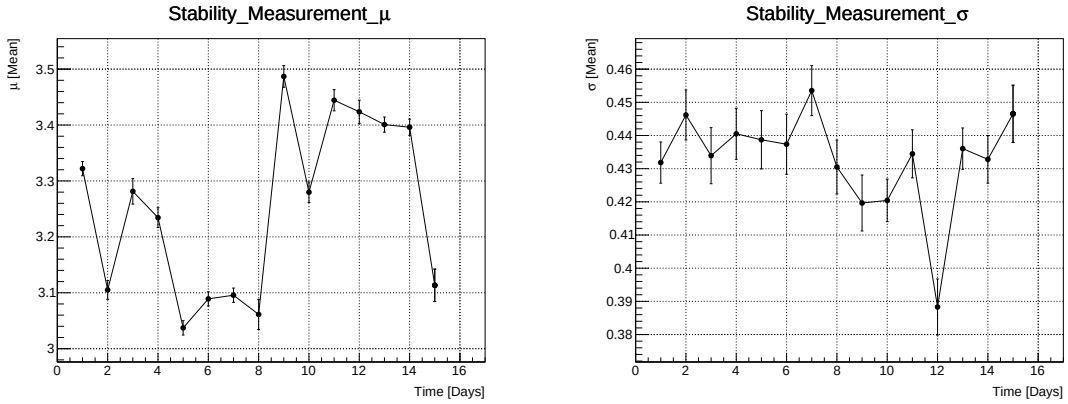


Figure 24: Result for threshold μ and noise σ of the VpedBias optimization.

It can be concluded that the threshold can vary up to $\pm 0.22\,\mathrm{mV}$ on a daily basis within the extend of this measurement. This explains the observed threshold difference.
A possible cause for these fluctuations could be temperature changes within the laboratory or the noise on the signal.

4.6 TRGbias

TRGbias controls the bias voltage of the trigger comparator. The parameter is studied between 900 - 2500 DAC–counts with a step size of 200 using the PMTref4–TRG_Thres scan. A sample of the remaining measurements can be found in appendix A.3.4.

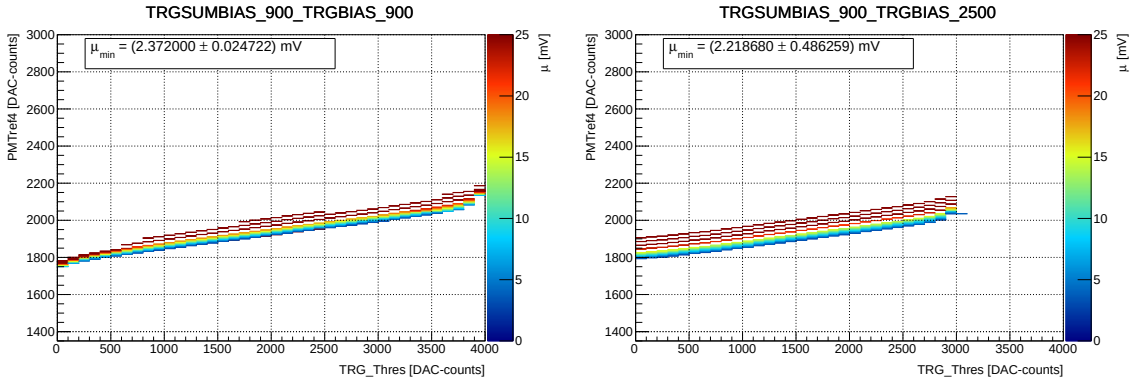


Figure 25: PMTref4–TRG_Thres Scan for TRGbias = 900 and 2500.

For high TRGbias values no more triggers are found after a specific value for TRG_Thres (see Figure 25). This is mainly due to the fact that high parameter values for TRGbias are no longer considered nominal. At this point some transistors within the trigger–comparator are operated outside their specifications [24]. Thus, it is difficult to predict the behavior of the trigger comparator for high TRGbias values.

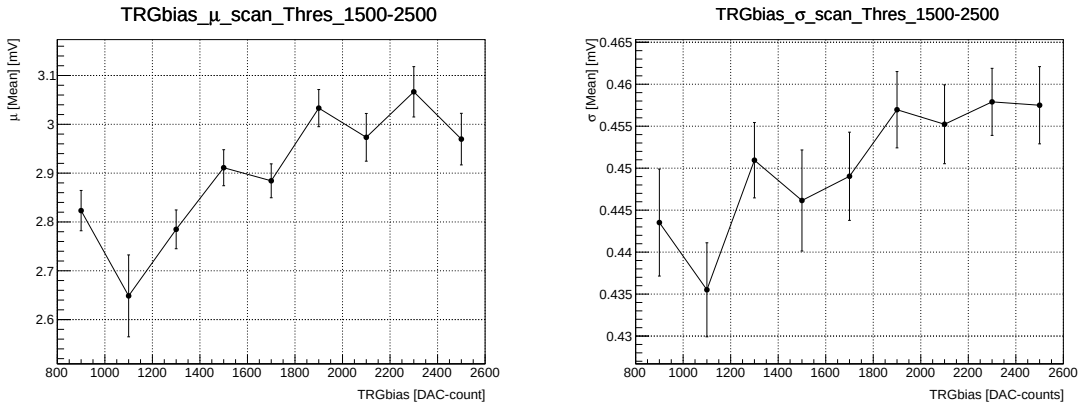


Figure 26: Result for threshold μ and noise σ of the TRGbias optimization.

Taking into account the default value for TRGbias (1000), the results shown in Figure 26 offer no significant improvement with regard to the error. Also a low value offers better power consumption. Thus, the default value for TRGbias is maintained.

4.7 TRGGbias

TRGGbias controls the gain of the first amplification of an incoming signal. Again the parameter is studied between 900 - 2400 DAC–counts using the established PMTref4–TRG_Thres scan with the TRG_Thres interval restricted to the region of interest (1500−2500 DAC–counts). For a better demonstration of the measurement fluctuation, the measurement was carried out twice. Important scans can be found in the appendix A.3.5.

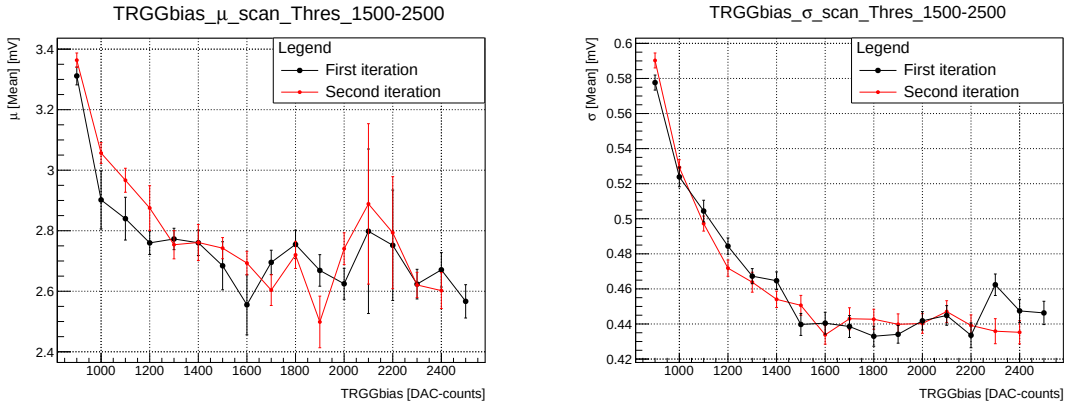


Figure 27: Result for threshold μ and noise σ of the TRGbias optimization.

For small TRGGbias values the amplification of the input signal is not sufficient. As a result, the signal–to–noise[11] ratio (SNR) decreases. Thus, a higher input signal amplitude

[11] Board internal noise and signal noise amplified by the amplifier.

is required to achieve the desired trigger behavior. This raises the measured threshold as observed in the Figure above.

When TRGGbias is increased and no signal is applied, random noise gets amplified. This leads to a higher initial PMTref4 start value (compare chapter 4.2.2). This can be seen in Figure 42 (appendix A.3.5).
The results in Figure 27 suggest to use higher parameter values. Note that there is no significant change in the noise or threshold for values bigger than 1600 DAC–counts. TRGGbias can therefore be reduced from its default value 1900 to 1600. This also allows a reduction in power consumption (see chapter 4.1).

4.8 TTbias

TTbias controls the supply bias for PMTref4 and TRG_Thresh for each trigger group. The parameter is studied between 900 - 2000 DAC–counts using the established PMTref4–TRG_Thres scan. This measurement was also carried out twice. In the second iteration of the measurement, only parameters up to 1700 DAC–counts were measured. The important scans can be found in the appendix A.3.6.

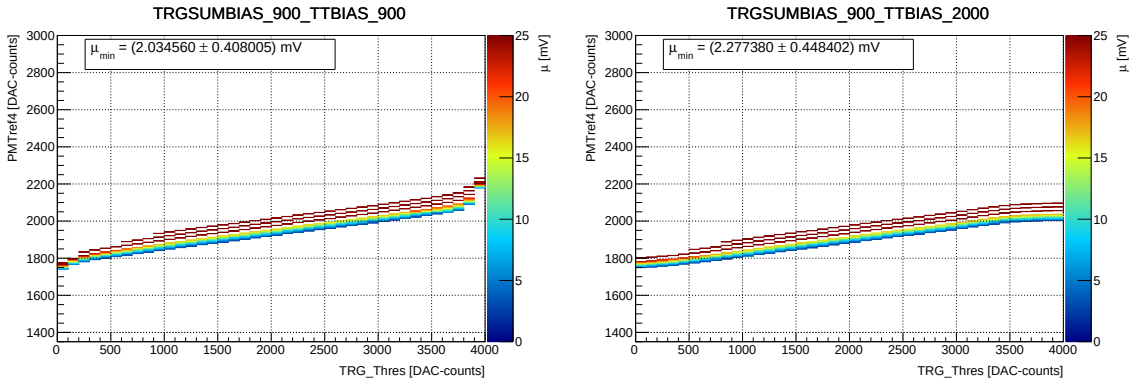


Figure 28: PMTref4–TRG_Thres scan for TTbias = 900 and 2000.

As it can be seen in Figure 28 the graph flattens out for low and high values of TRG_Thres. This parameter further reduces non–linear behavior of PMTref4 to the point where the linear–range of TRG_Thres becomes apparent.
Because the voltage of TRG_Thres is produced by a DAC, its transfer function looks akin to Figure 12. Outside the linear–range, a big adjustment in TRG_Thres may only lead to a small change in the output voltage produced by the DAC–count set for TRG_Thres. Thus, leading to the flattening observed in Figure 28.
In Figure 29 it can be seen that the choice of the parameter value does not matter considering the error. Thus, the default value 1100 is again maintained.

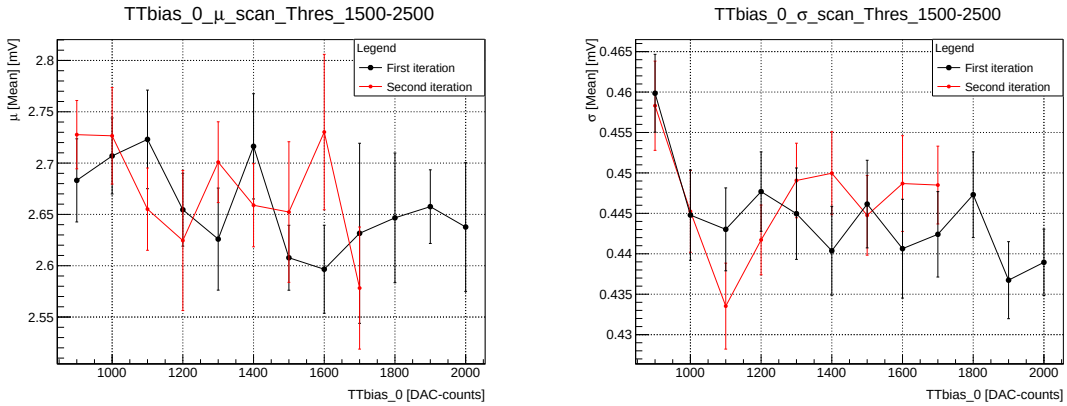


Figure 29: Result for threshold μ and noise σ of the TTbias optimization.

4.9 TTbias_C

TTbias_C controls the supply bias for VpedBias, TRGbias, TRGsumbias and TRGGbias. Therefore, a change in TTbias_C will influence all previous parameters. It is studied between 900 - 2200 DAC–counts. The PMTref4–TRG_Thres scan was again conducted twice. Important scans of the second iteration can be found in A.3.7.

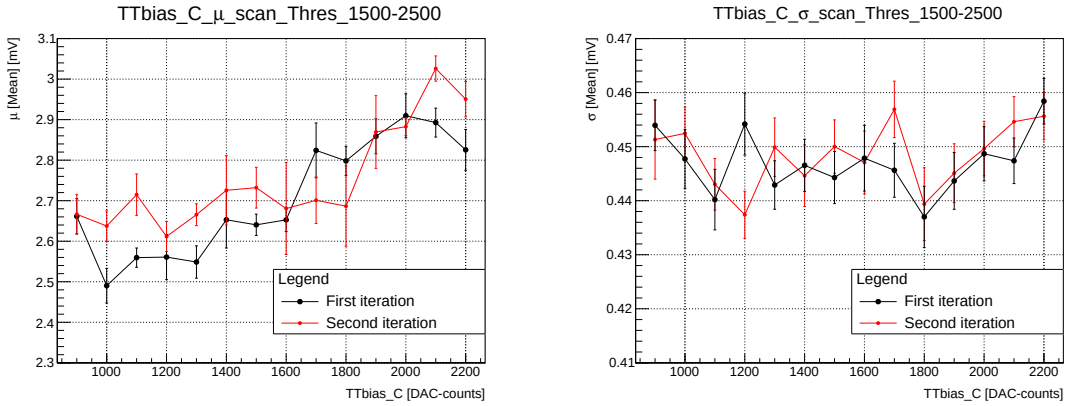
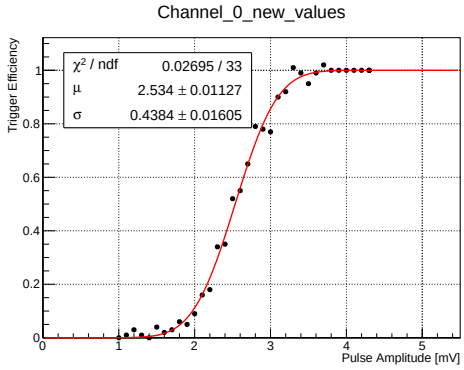


Figure 30: Result for threshold μ and noise σ of the TTbias_C optimization.

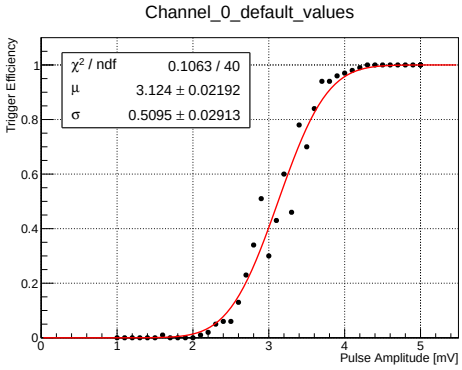
As it can be seen in Figure 30 above, the default value 1000 is a good choice in terms of threshold and noise as well as power consumption. Thus, the default value is maintained.

5 Conclusion

Considering the performed measurements, it can be concluded that the previously used default values for the T5TEA parameters have already been nearly optimal.
However, the results of the performed analysis suggest that TRGsumbias should be changed from 2400 to 900 DAC–counts (see chapter 4.4) and TRGGbias from 1900 to 1600 DAC–counts (see chapter 4.7).
A comparison between the lowest thresholds for the default values and new values has been made using a trigger–efficiency measurement[12]. The results in Figure 31 show, that the new parameters provide lower noise and threshold values while also lowering the current draw (heat development) due to the lower parameter values.



(a) Trigger–efficiency for optimized values (TRG_Thresh = 2200, PMTref4 = 1825).



(b) Trigger–efficiency for default values (TRG_Thresh = 2974, PMTref4 = 1980).

Figure 31: Side by side comparison between the trigger–efficiency.

The new parameters are, unlike the default ones, within the linear section of the PMTref4–TRG_Thres scan. It should also be noted, that the used function generator has not been calibrated in a long time and applied amplitudes are at least 10 % smaller than the set value. Thus, the true thresholds are even lower than shown here in this thesis.
Taking all of this into account, T5TEA is well within the requirements set by the CTA consortium (see chapter 3).

Furthermore, the long-term study of noise and threshold for constant parameters has yielded a fluctuation up to ±0.22 mV on a daily basis.

[12] Both measurements were performed in sequence to minimize the effect of time dependent fluctuations.

6 Outlook

As seen in chapter 4.4, there is a temperature dependency of T5TEAs trigger behavior. However, the exact relation between threshold, noise and temperature is not yet understood. Thus, T5TEA could be placed in a thermal chamber under constant environmental conditions, to further understand its temperature response.
Also lower thresholds were observed, when the TC was disabled. Therefore, further analysis of interferences caused by TC would be beneficial.

Since many of the parameters considered in this thesis are interdependent, future measurements with another arrangement of these parameters could yield even better results.
Additionally, in the scope of this thesis not all parameters of T5TEA and only one of the 16 input channels were considered. Thus, further investigation is needed to fully optimize T5TEAs parameters.

A Appendix

A.1 Default values

All measurements were conducted using the so called default values. When better values are found, they are used instead when not stated otherwise.

Parameter	Value [DAC–counts]
VpedBias	1800
Vped_0	1000
TRGsumbias	2400
TRGbias	1000
TRGGbias	1900
TTbias_0	1100
TTbias_C	1000
TTbias_A	400

Table 1: Default values used if nothing else is mentioned or no better values are found.

A.2 Power consumption

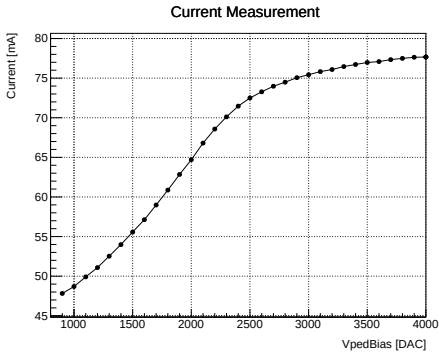


Figure 32: Current draw of T5TEA for default values and variable VpedBias.

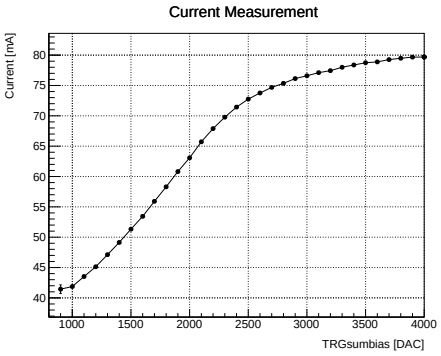


Figure 33: Current draw of T5TEA for default values and variable TRGsumbias.

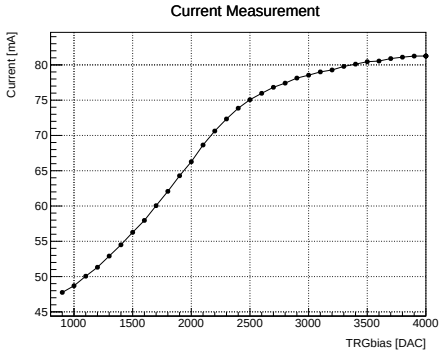


Figure 34: Current draw of T5TEA for default values and variable TRGbias.

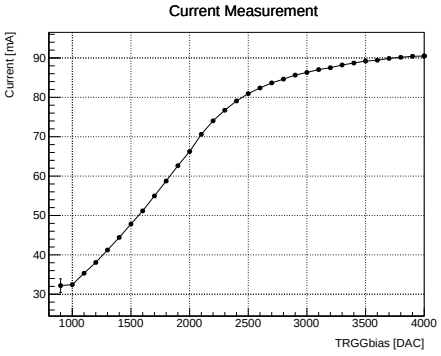


Figure 35: Current draw of T5TEA for default values and variable TRGGbias.

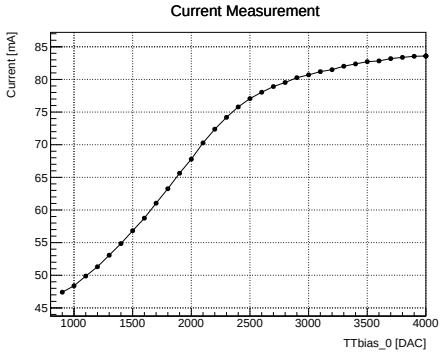


Figure 36: Current draw of T5TEA for default values and variable TTbias_0.

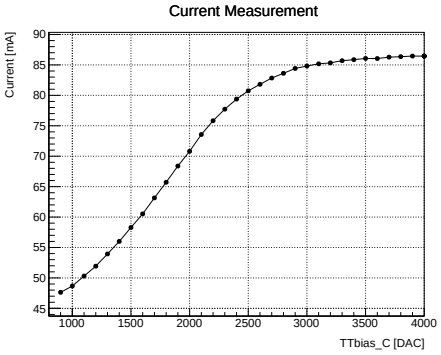


Figure 37: Current draw of T5TEA for default values and variable TTbias_C.

A.3 Parameter optimization

A.3.1 VpedBias

VpedBias [DAC–counts]	Vped [DAC–counts]	Deviation [mV]
1100	1023	2.3
1200	1023	1.2
1300	1022	0.1
1400	1018	0.2
1500	1014	0.2
1600	1010	0.1
1700	1006	0.3
1800	1000	0
1900	1000	3.0
2000	1000	6.3
2100	982	0.3
2200	976	0.2

Table 2: Found Vped value for a given VpedBias with offset voltage deviation with respect to the one measured for the default values (657.2 mV).

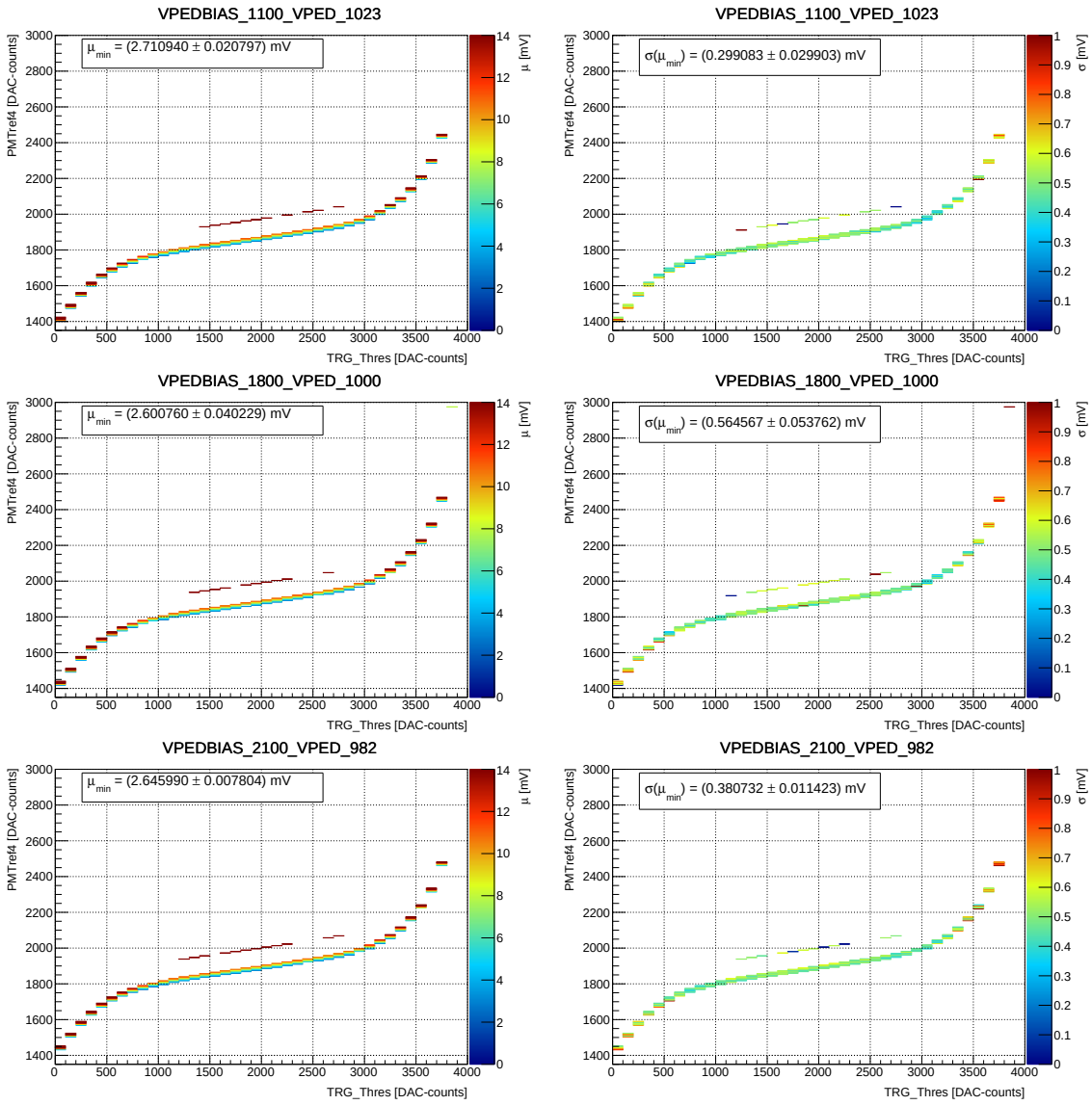


Figure 38: Samples of PMTref4–TRG_Thres scans for VpedBias.

A.3.2 Vped

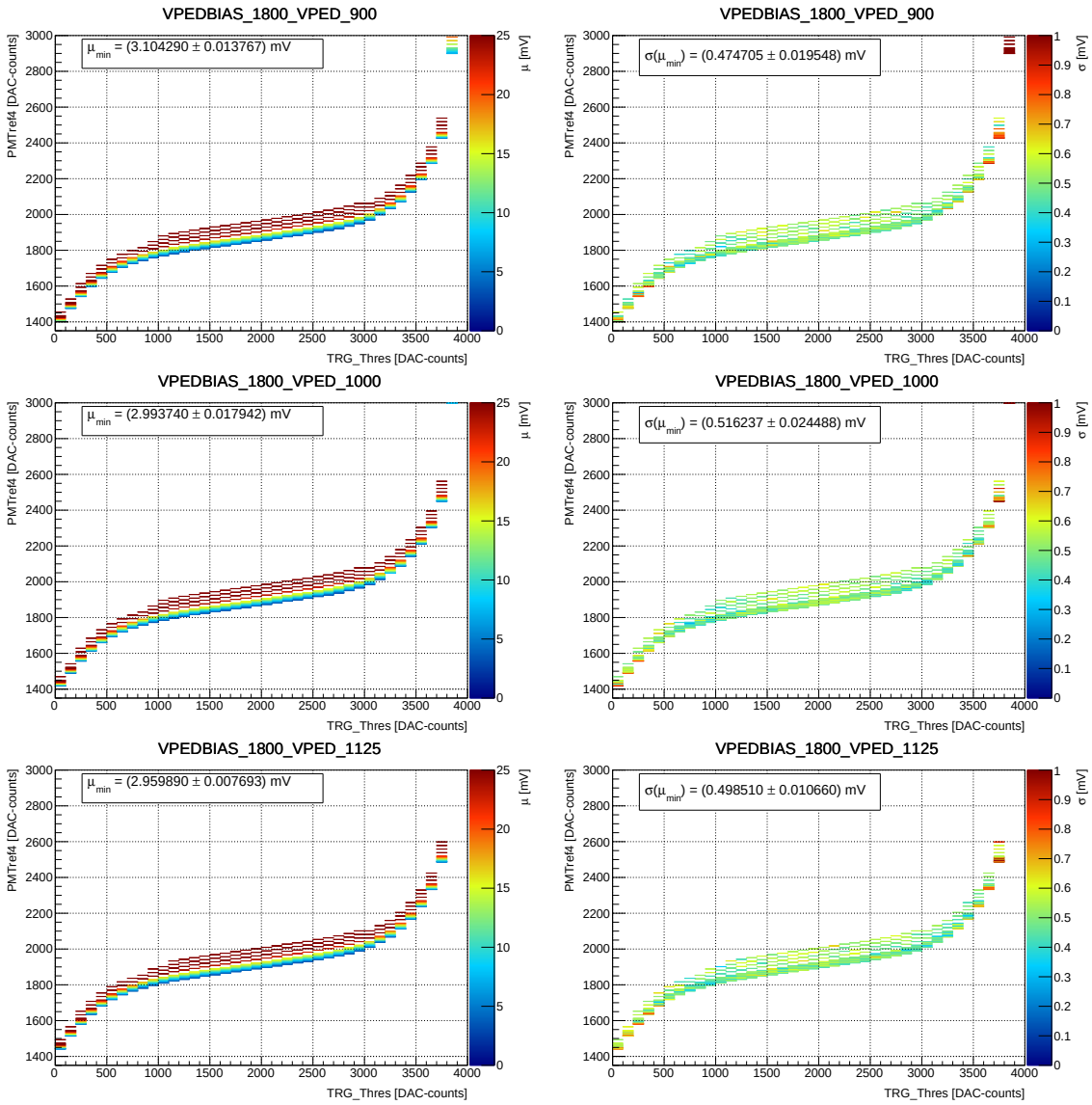


Figure 39: Samples of PMTref4–TRG_Thres scans for Vped.

A.3.3 TRGsumbias

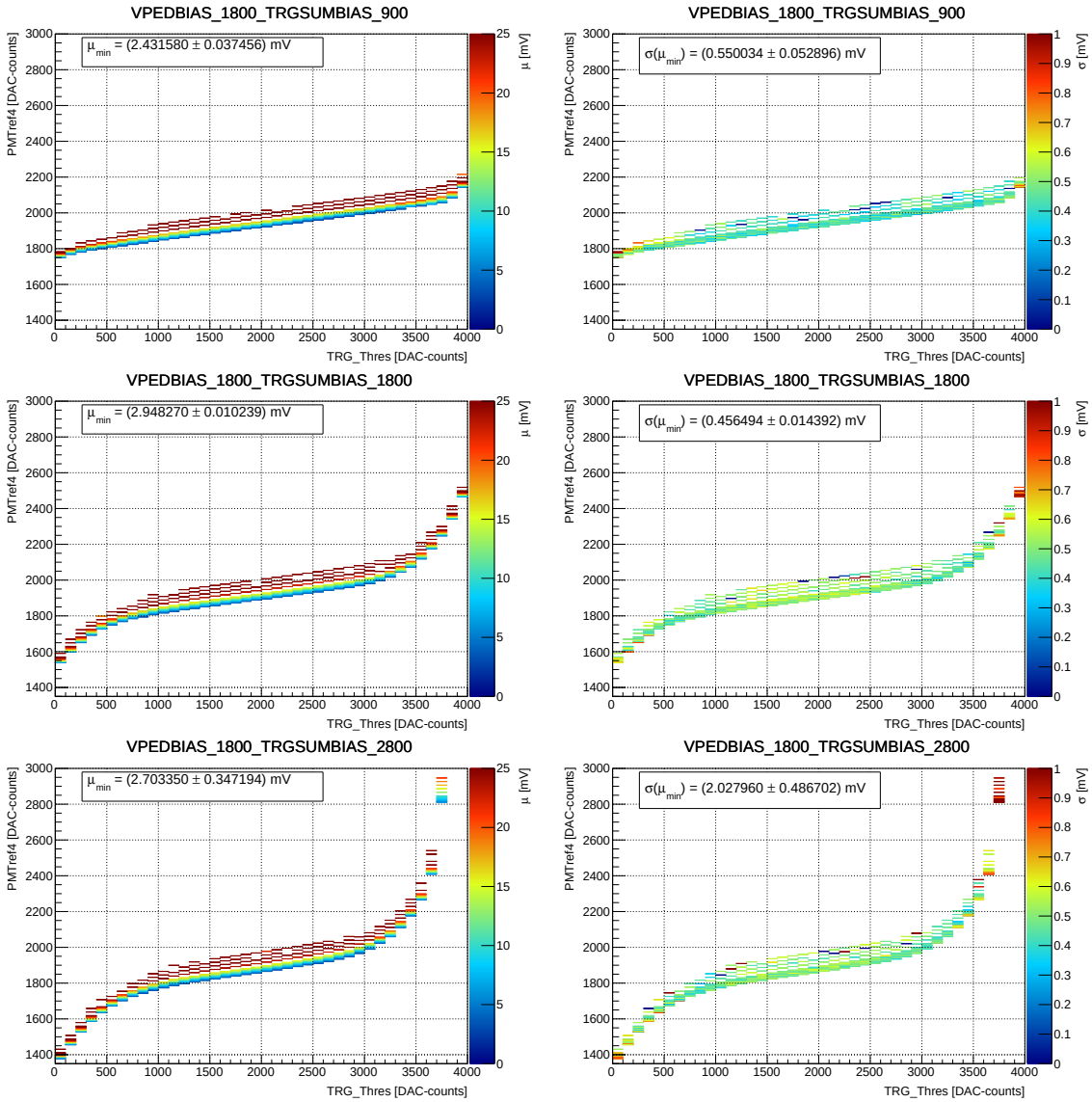


Figure 40: Samples of PMTref4–TRG_Thres scans for TRGsumbias.

A.3.4 TRGbias

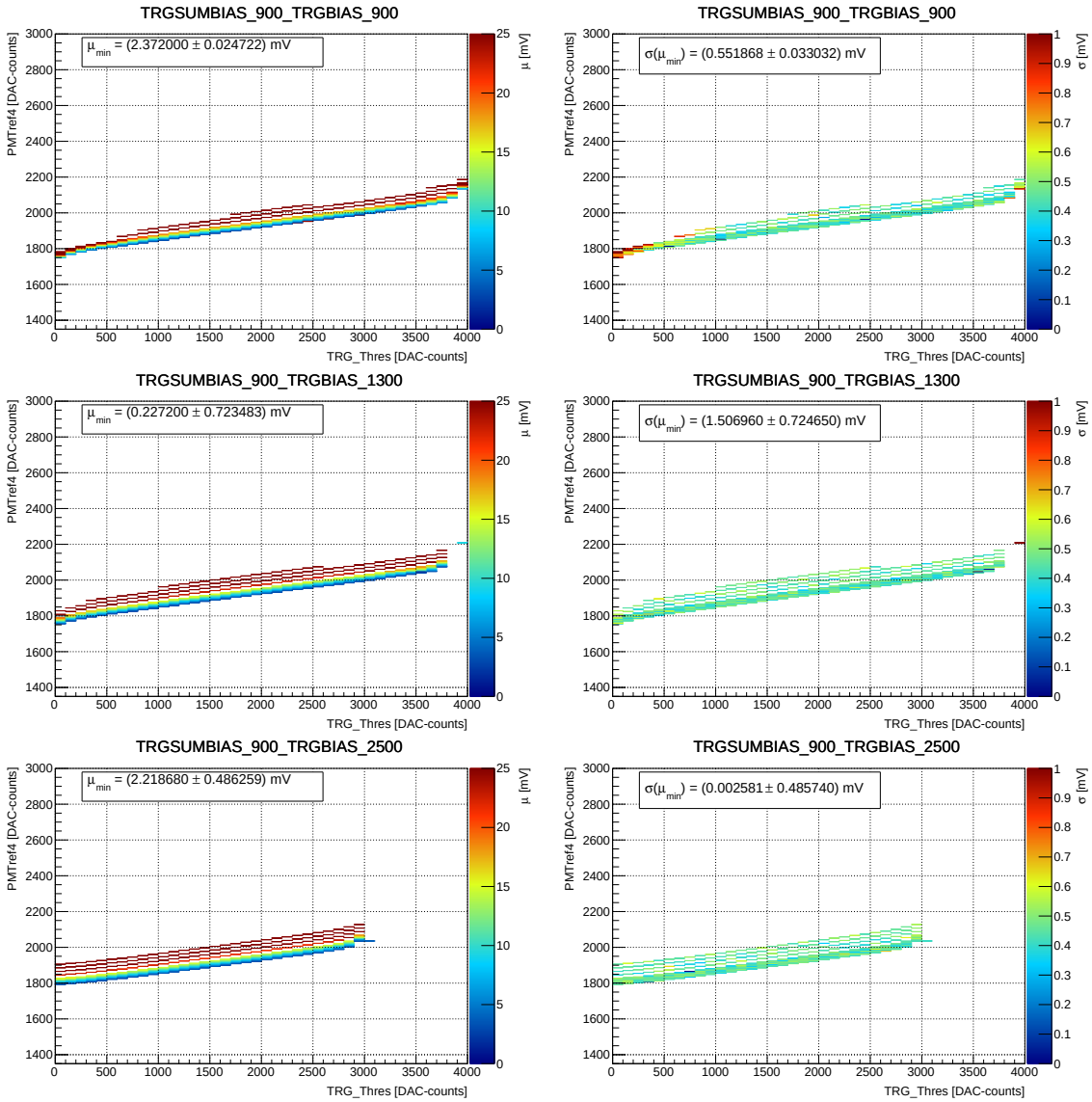


Figure 41: Samples of PMTref4–TRG_Thres scans for TRGbias.

A.3.5 TRGGbias

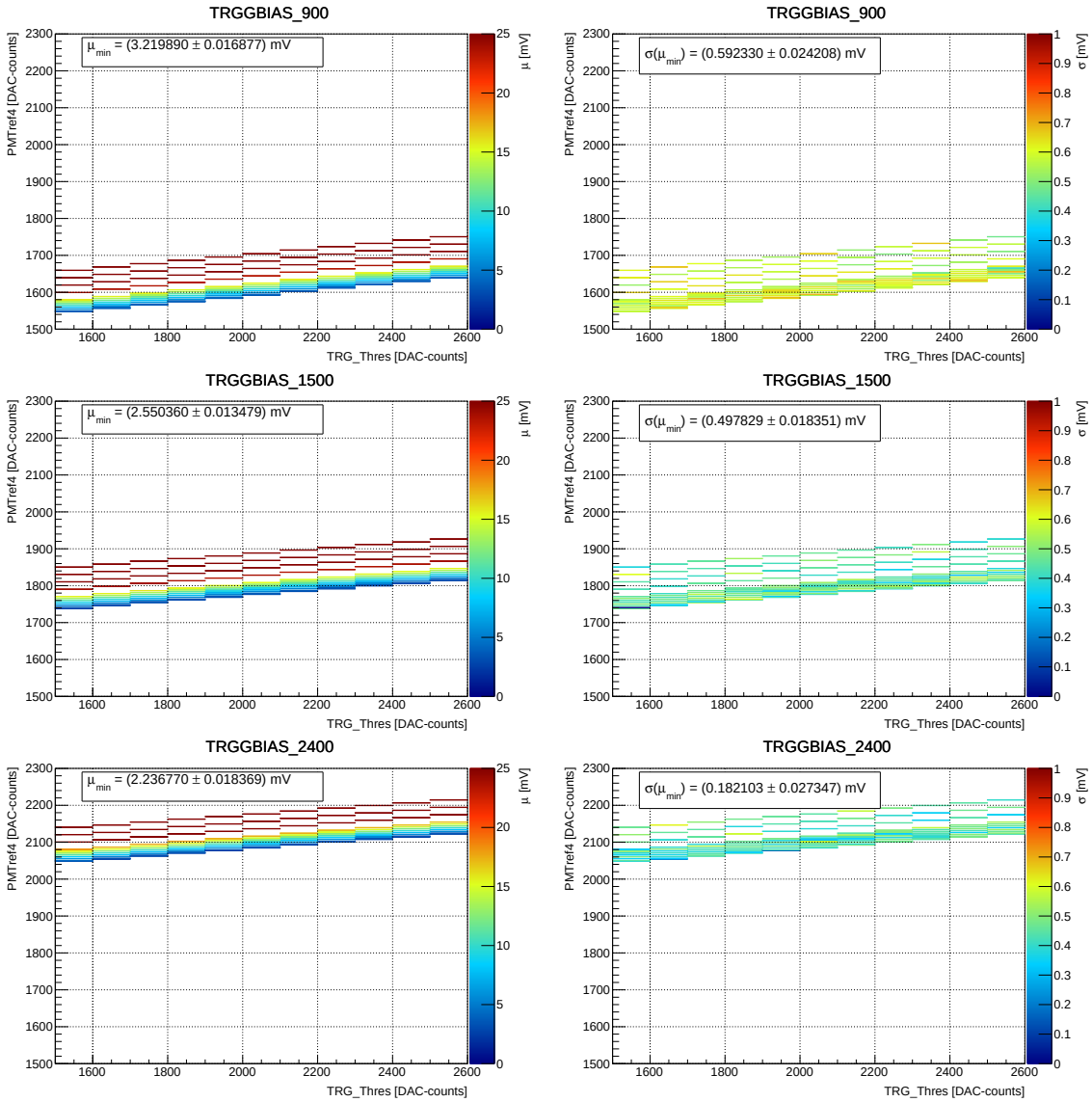


Figure 42: Samples of PMTref4–TRG_Thres scans for TRGGbias.

A.3.6 TTbias

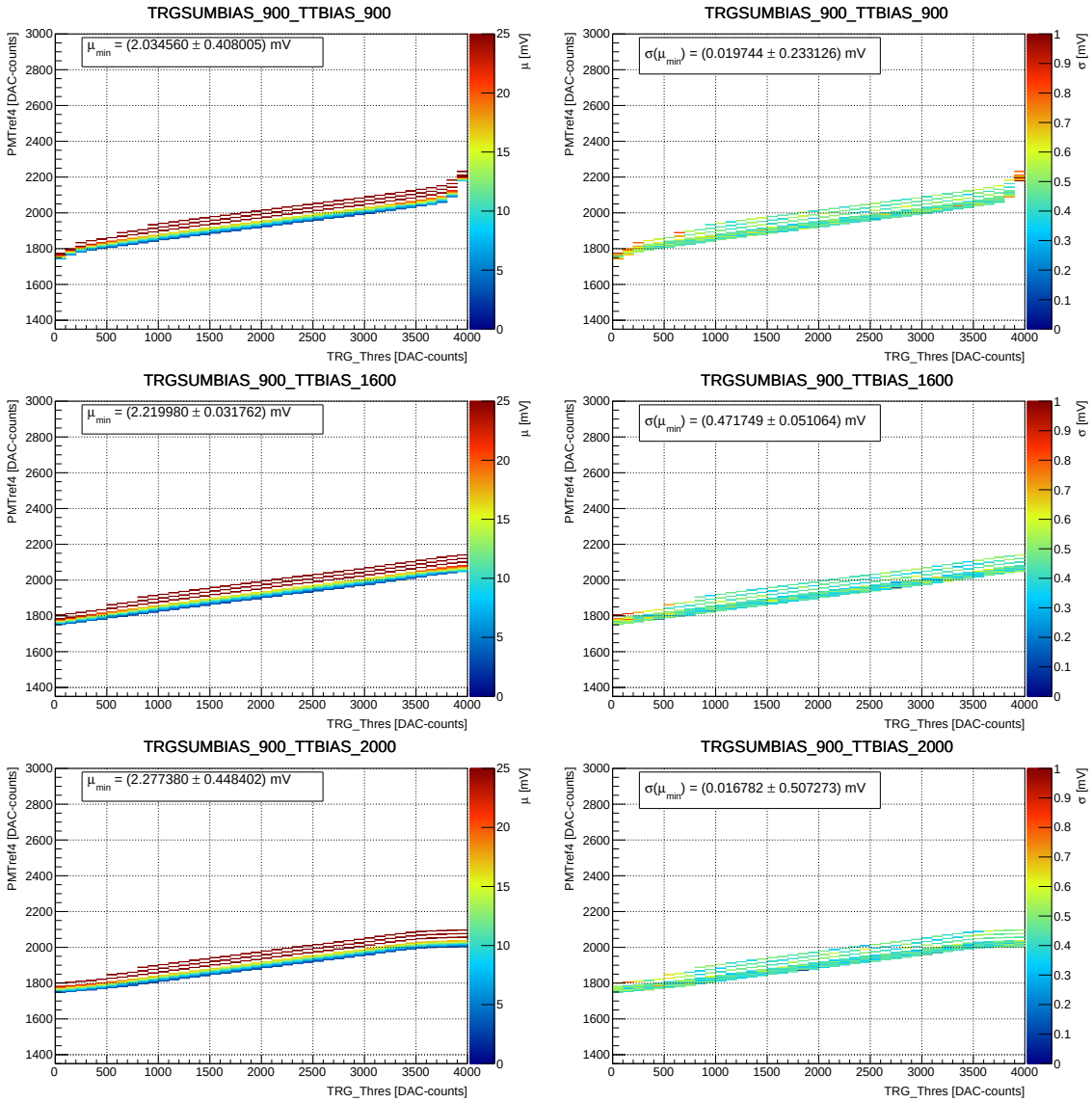


Figure 43: Samples of PMTref4–TRG_Thres scans for TTbias.

A.3.7 TTbias_C

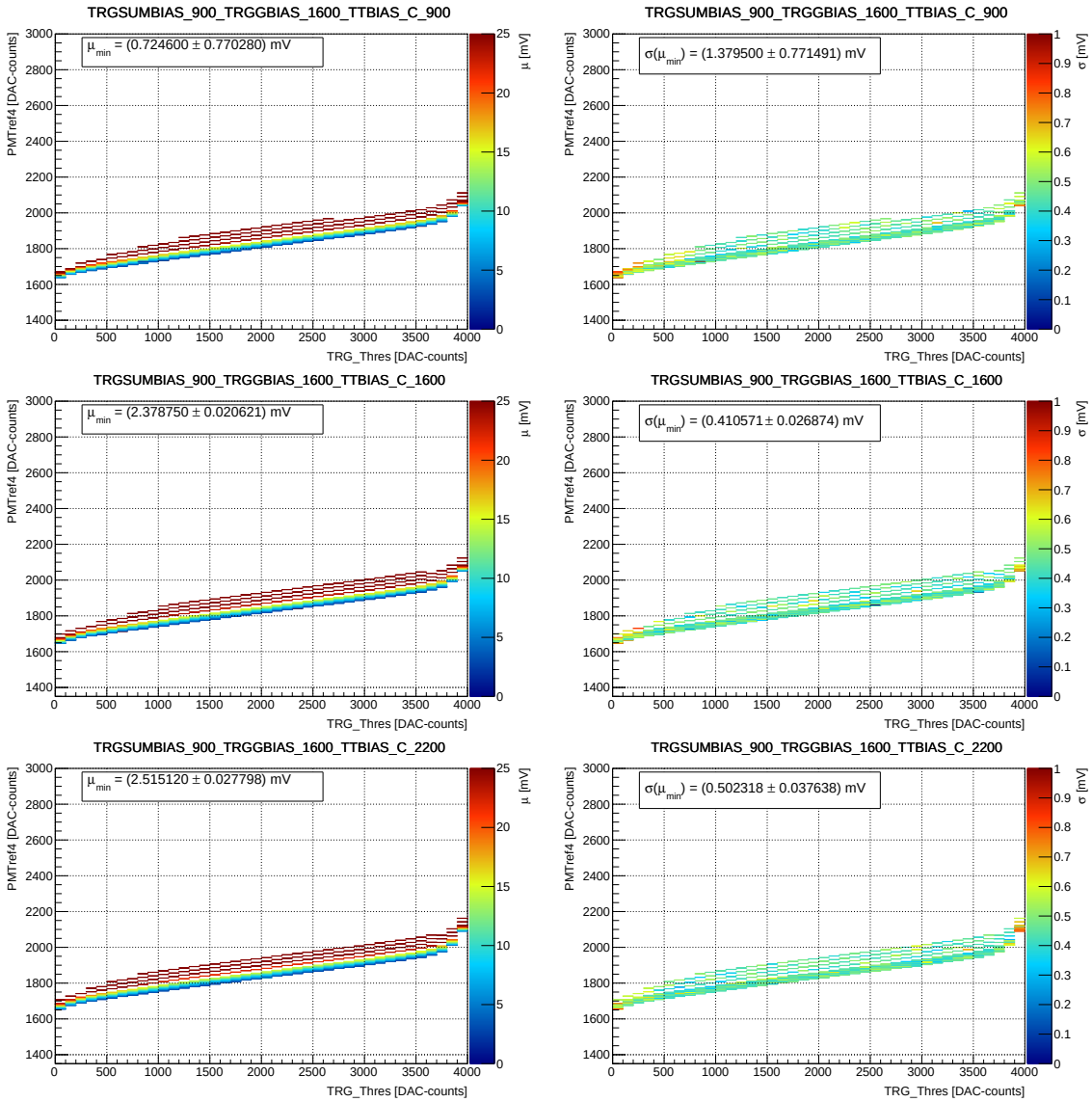


Figure 44: Samples of PMTref4–TRG_Thres scans for TTbias_C.

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[1] Wikipedia from 12th December 2016, Created by Ruben Castelnuovo, Copyright information: CC BY-SA 3.0. https://upload.wikimedia.org/wikipedia/commons/0/08/Utube.PNG.

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Danksagung

An dieser Stelle möchte ich mich bei allen bedanken, die es mir ermöglicht haben diese Arbeit erfolgreich abzuschließen und mir Unterstützung geleistet haben. Insbesondere gilt mein Dank hierbei:

- **Prof. Dr. Stefan Funk** für die Vergabe dieses interessanten Themas.
- **Prof. Dr. Gisela Anton** für die Übernahme des Zweitgutachtens.
- **Adrian Zink** für seine Geduld mit mir, die Betreuung während der Arbeit und für das Korrekturlesen.
- **David Jankowsky** für die sehr nützlichen Tipps zu meiner Arbeit und das Korrekturlesen.
- **Jacqueline Catalano** für das Korrekturlesen und die hilfreiche Unterstützung während der Arbeit, gerade in der Anfangsphase.
- **Meinen Kollegen** und der Arbeitsgruppe für die super Arbeitsatmosphäre und zahlreiche lustige Momente.
- **Laura Herold** und **Peter Deiml** für das Korrekturlesen.
- **Meiner Familie** für die Unterstützung während meines gesamten Studiums, die Geduld mit mir und dass sie immer ein offenes Ohr für meine Probleme haben.
- Meinem Freund, **Florian Iglhaut**, für den Beistand während dieser Arbeit und das Aufmuntern in stressigen Situationen.
- **Udo Schmidt** und **Daniel Fischaleck** für Rechtschreib- und Grammatiküberprüfung.

Erklärung

Hiermit bestätige ich, dass ich diese Arbeit selbstständig und nur unter Verwendung der angegebenen Hilfsmittel angefertigt habe.

Erlangen, den 15. 12. 2016